REMARKS

Claims 1, 7 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Balasubramanian et al. (U.S. Patent No. 5,767,004). Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Balasubramanian and in view of Yu et al (U.S. Patent No. 6,225,167). Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Balasubramanian. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Balasubramanian '004 and in view of Applicant admitted prior art. Claims 9-12 and 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu '167 in view of Balasubramanian '004. Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Balasubramanian '004 and Yu '167 and in view of Hayakawa (U.S.Patent No. 5,779,520).

1. Claims 1-8 and 17 are rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant(s) regard as their invention. Evidence that claims 1-8 and 17 fail(s) to correspond in scope with that which applicant(s) regard as the invention can be found in specification originally filed March 25, 2002. In that paper, applicant has stated "contaminants adhering to the semiconductor wafer 100 **are removed**"(see [0025]); "the present invention shows marked improvement in **preventing the occurrence of particles and defects** of various shapes and sizes" (see [0030]), and this statement indicates that the invention is different from what is defined

in the claims(s) because claim 2 recites: "the surface of the semiconductor wafer **comprising a plurality of particles**" (lines 2-3).

Response:

In the AMENDMENT filed July 4, 2003 which has been entered as Paper No.3, the term "which utilizes the particles on the surface of the semiconductor wafer" in claim 1 is changed to "which growing by way of the particles on the surface of the semiconductor wafer". The amended portion is disclosed in the specification on page 7, lines 18-21. No new matter is included.

Actually, contaminants adhering to the semiconductor wafer 100 are removed by a wet etching process and a wet cleaning process performed after removing the photoresist layer (see [0025]). Although most of the contaminants, such as organic contaminants, particles, metallic contaminants, adhering to the semiconductor wafer 100 are removed, however, it is impossible to remove all of the contaminants with the now existing semiconductor technique. Therefore, the surface of the semiconductor wafer **comprises a plurality of particles** (lines 2-3), which cannot be removed by the wet etching process and the wet cleaning porcess. After that, a two-step low pressure chemical vapor deposition process is used to form the first amorphous layer 116a and the second polysilicon layer 116b together form the first polysilicon layer 116. The advantage of the two-step polysilicon deposition process according to the present invention is that depositing with a low temperature first, in which the

crystallinity is not marked, tends to form an amorphous silicon (α -Si) structure. Nucleation is thus effectively inhibited to further avoid grains growing by way of small and large particles on the surface of the semiconductor wafer during crystallization, which would otherwise result in the occurrence of protrusions and defects as shown in Fig.6. Finally, the present invention shows marked improvement in preventing the occurrence of particles and defects of various shapes and sizes" (see [0030]).

Owing to the process sequence mentioned above, the Applicant believes that claims 1-8 and 17 do not fail to correspond in scope with that which applicant(s) regard as the invention can be found in specification originally filed March 25, 2002. Reconsideration of the rejection over claims 1-8 and 17 is hereby requested.

2. Claims 1-8 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites: "the surface of the semiconductor wafer **comprising a plurality of particles**" (lines 2-3).

Please note: prior to performing two-step deposit, the semiconductor wafer have been cleaned by: megasonic scrubbing, SC-1 and SC-2 clean. ([0025]). Therefore, all particles (contaminants adhering the semiconductor wafer; organic contaminants and particles and metallic contaminants) have been removed.

(See [0025]).

Therefore, the preamble of claim 1 clearly lacks support from the specification.

Where are those "plurality of particles" came from since the wafer have been thoroughly clean?

With respect to claim 5, Applicant asserted that "the term particles means the already existing particles on the surface of the semiconductor wafer before performing the two-step silicon deposition process'.

As clearly discussed above, prior to the two-step deposition, the semiconductor wafer has been thoroughly wet cleaned (megasonic, SC-1 and SC-2) to remove the particles. ([0025]).

With respect to claim 17, the limitation of claim 17 includes: wherein the defects comprises needle-like defects".

While claim 9, which claim 17 depends-on, recites: "wherein the two-step silicon deposition process comprises a first step low temperature amorphous silicon (α-Si) deposition process **to avoid formation of particles and defects by inhibiting nucleation…**"

Therefore, claim 17 is contrary to claim 9, because the formation of the defects have been avoided by the formation of the amorphous silicon layer.

What is the shape of the particles that does not exist?

Please note: the needle-like defects only exists if the amorphous silicon have not been formed (See Fig.6, page 4, [0013-0014]).

Response:

Please refer to the response to the rejection over claims 1-8 and 17 under 35 U.S.C. 112 (item 1), although most of the contaminants, such as organic contaminants, particles, metallic contaminants, adhering to the semiconductor wafer 100 are removed by the wet etching process and the wet cleaning process, **it is impossible to remove all of the contaminants with the now existing semiconductor technique.** The surface of the semiconductor wafer thus **comprises a plurality of particles** (lines 2-3). Therefore, the preamble of claim 1 does not lack support from the specification.

In claims 5, the term "particles" means the plurality of particles comprised on the surface of the semiconductor wafer because **it is impossible to remove all of the contaminants with the now existing wet etching and set cleaning processes.** As a result, the term particle means the already existing particles on the surface of the semiconductor wafer, which cannot be removed by the wet etching and wet cleaning processes, before performing the two-step silicon deposition process.

In claim 9, the term "the two-step silicon deposition process comprises a first step low temperature amorphous silicon (α -Si) deposition process to avoid formation of **particles and defects** by inhibiting nucleation during the formation of the polysilicon layer, and a second step high temperature polysilicon deposition process." means that the formation of the particles have been avoided by the formation of the amorphous silicon layer **as possible.**

As shown in Fig.14, a small quantity of particles still exist on the semiconductor wafer 100 after forming the first gate 118 and the second gate 122 since **it is impossible to remove all of the contaminants with the now existing wet etching and wet cleaning processes. Therefore, a small quantity of particles still exists on the surface of the semiconductor wafer before performing the two-step silicon deposition process to result in particles of various shapes and sizes after forming the first gate 118 and the second gate 122.**

According to the present application, the two-step silicon deposition process comprises a first step low temperature amorphous silicon (α -Si) deposition process used for inhibiting nucleation so as to avoid formation of defects. **In claim 17, the Applicant wants to point out that the formation of the needle-like defects is avoided.**

Therefore, the Applicant believes that claims 1-8 and 17 do not fail to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Reconsideration of the rejection over claims 1-8 and 17 is hereby requested.

3. Claims 1, 7 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Balasubramanian et al. (U.S. Patent No. 5,767,004) of record.

With respect to claim 1, as best understood by the examiner, Balasubramanian teaches a method for making a polysilicon film on a semiconductor wafer, the method comprising:

performing a two-step silicon deposition process, the two-step silicon deposition process comprising:

a first step amorphous silicon (16) deposition process utilizing a low temperature; and

a second step polysilicon (18) process utilizing a high temperature (See Fig.1, col.1-12).

With respect to the functional limitation of the two-step deposition process: 'wherein the first step amorphous silicon (α-Si) deposition process is used to avoid nucleation of the polysiliocn film growth, which growing by way of the particles on the surface of the semiconductor wafer, so as to inhibit occurrences of needlelike particles and defects on the surface of the polysilicon film", since the deposition process of Balasubramanian is performed by two-step silicon deposition as claimed, thus "avoiding nucleation of the polysilicon film growth, which growing by way of the particles on the surface of the semiconductor wafer so as to inhibit occurrences of needlelike particles and defects on the surface of the polysilicon film" is an inherent result of the two-steps silicon deposition.

With respect to claim 7, the polysilicon layer (18) of Balasubramanian is deposited at the temperature that includes the claimed range.

With respect to claim 8, the two-step silicon deposition process of Balasubramanian is performed in a single wafer type LPCVD equipment.

Note that, until proven otherwise, the LPCVD equipment of Balasubramanian includes single wafer type LPCVD equipment.

Response:

First, the Applicant intends to point out the difference between claim 1 of the present application and Balasubramanian's disclosure. Claim 1 of the present application is repeated below:

1. A method for making a polysilicon film on a semiconductor wafer, the surface of the semiconductor wafer comprising a plurality of particles, the method comprising:

performing a two-step silicon deposition process, the two-step silicon deposition process comprising:

a first step amorphous silicon (α -Si) deposition process utilizing a low temperature; and

a second step polysilicon deposition process utilizing a high temperature;

wherein **the first step amorphous silicon (α -Si) deposition process is used to avoid nucleation of the polysilicon film growth, which growing by way of the particles on the surface of the semiconductor wafer, so as to inhibit occurrences of needle-like particles and defects on the surface of the polysilicon film.**

As disclosed in claim 1 of the present application, there is one obvious difference between Balasubramanian's invention and the present application. According to Balasubramanian's invention, the deposition temperature of the amorphous silicon layer is 500 to 580°C, and the deposition temperature of the polysilicon layer is 600 to 700°C. In the present application, a temperature of the first step amorphous silicon deposition process ranges from 550 to 650°C,

and a temperature of the second step polysilicon deposition process ranges from 680 to 710°C. **Although the ranges of the d position temperatures of Balasubramanian's invention somewhat overlap with the ranges of the deposition temperatures of the present application, the deposition temperatures of the present application are obviously higher than the deposition temperatures of Balasubramanian's invention.**

The reason why the deposition temperatures of the present application are obviously higher than the deposition temperatures of Balasubramanian's invention is that a subsequent anneal process is necessary in Balasubramanian's invention. According to Balasubramanian's invention, an anneal process is taught to form a low impurity diffusion polysilicon layer. **By simultaneously performing the annealing process to a formed amorphous silicon layer and a polysilicon layer, a polysilicon multi-layer with grain boundary mis-matched polycrystalline properties is formed.** With the grain boundary mis-matched polycrystalline properties, inter-diffusion of impurities are inhibited to result in the low impurity diffusion polysilicon layer. **In other words, Balasubramanian never teaches how to form a polysilicon layer by only utilizing a two-step silicon deposition process. Rather, two deposition processes having obviously lower deposition temperatures than the deposition temperatures of the present application are utilized by Balasubramanian and an annealing process is nec ssary in Balasubramanian's invention.**

In addition, Balasubramanian **never teaches how to utilize a first step amorphous silicon deposition process to inhibit occurrences of needle-like contamination** on the surface of the final formed polysilicon film. In the present application, **even though originally the surface of the semiconductor wafer comprises a plurality of particles**, the occurrences of needle-like contamination on the surface of the final formed polysilicon film are inhibited **because the first step amorphous silicon deposition process can avoid nucleation of the polysilicon film growth by way of the particles on the surface of the semiconductor wafer.**

From the above discussion, the Applicant believes that claim 1 of the present application is absolutely different from Balasubramanian's disclosure. Reconsideration of the rejection over the amended claim 1 is hereby requested.

As claims 7-8 are dependent upon claim 1, they should be allowed if claim 1 is allowed. Reconsideration of the rejection over claims 7-8 is therefore requested.

4. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Balasubramanian '004 as applied to claim 1 above, and further in view of Yu et al. (U.S. Patent No. 6,225,167).

With respect to claim 2, Balasubramanian teaches a method of making a polysilicon film on a

semiconductor wafer including performing a two-step silicon deposition process.

Thus, Balasubramanian is shown to teach all the features of the claim with the exception of disclosing the process performing before the two-step silicon deposition process.

However, Yu teaches the process performing prior to making conductive gate electrodes including: at least one photolithography process, one wet etching process, one photoresist stripping process, one wet cleaning process and one thermal oxidation process are performed on the surface of the semiconductor wafer(200).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to before performing the two-step silicon deposition process of Balasubramanian performing the processes as taught by Yu to form the gate oxide for the silicon gate electrodes,

With respect to claim 3, as best understood by the examiner, the wet etching process of Yu comprises a buffer oxide etchant (BOE) etching process and followed by SC-1 cleaning process.

Response:

As claims 2-3 are dependent upon claim 1, they should be allowed if claim 1 is allowed. Reconsideration of the rejection over claims 2-3 is therefore requested.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Balasubramanian '004.

Balasubramanian teaches the first step amorphous (16) is deposited at a temperature range (500 to 580 °C) that overlaps the claimed range (550 to 650°C) and at a thickness of about 400Å.

Thus, Balasubramanian is shown to teach all the features of the claim with the exception of explicitly forming a thinner amorphous layer (100 Å). Note that, the claimed thickness does not appear to be critical.

Note that the specification contains no disclosure of either the *critical nature of the claimed thickness, 100 Å, of any unexpected results arising therefrom.* Where patentability is aid to based upon particular chosen dimension or upon another variable recited in a claim, the Applicant must show that the chosen dimension are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir 1990).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the amorphous silicon film of Balasubramanian to a thickness that able to create a grain boundary mis-matched, thus, forming a low impurity diffusion gate electrode.

Response:

As claim 6 is dependent upon claim 1, it should be allowed if claim 1 is allowed. Reconsideration of the rejection over claim 6 is therefore requested.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Balasubramanian '004 as applied to claim 1 above, and further in view of Applicant admitted prior art.

As best understood by the examiner, Balasubramanian is shown to teach all the features of the claim with the exception of disclosing any contaminants if existed prior to the deposit of the amorphous silicon layer (16).

However, the admitted prior art teaches that there are many contaminants exited in a semiconductor process including: particles, organic substance, micro-defects and metal particles adhering to the wafer (See [0006]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to includes the particles in the semiconductor wafer of Balasubramanian as taught by the admitted prior art because the particles should not be detrimental to the process since they would have been removed by the wet cleaning process.

Response:

Please refer to the response to the rejection over claims 1-8 and 17 under 35 U.S.C. 112 (item 1), although most of the contaminants, such as organic contaminants, particles, metallic contaminants, adhering to the semiconductor wafer 100 are removed by the wet etching and wet cleaning processes, **it is impossible to remove all of the contaminants with the now existing semiconductor technique**. Therefore, the surface of the semiconductor wafer **comprises a plurality of particles** (lines 2-3).

In addition, as claim 5 is dependent upon claim 1, it should be allowed if claim 1 is allowed.

Reconsideration of the rejection over claim 5 is therefore requested.

7. Claims 9-12 and 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu '167 in view of Balasubramanian '004.

Yu teaches a method of forming a polysilicon film on a semiconductor wafer, a surface of the semiconductor wafer comprising a first gate oxide area (40) and a second gate oxide area (50), substantially as claimed including:

forming a first gate oxide layer (20) on the surface of the semiconductor wafer (10);

performing a photolithography process and an etching process to remove the first gate oxide layer (20) on the surface of the second gate oxide area (50);

performing a cleaning process; and performing a conductive gate electrodes deposition process covering he first gate oxide area (40) and the second gate oxide area (50) to form MOS transistors. (See Fig.1a-d, col. 1-10).

Thus, Yu is shown to teach all the features of the claim with the exception of explicitly disclosing the process of forming the conductive gate electrodes.

However, Balasubramanian teaches a process of forming conductive gate electrodes covering gate oxide including:

performing a two-step silicon deposition process to form a polysilicon layer (18), the polysilicon layer (18) covering the gate oxide layer (14); wherein the lower layer (16) of anosphous silicon is deposited at

a low temperature and the upper layer (18) of polysilicon is deposited at a high temperature. (See Fig.1, col.6, lines 33-67).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the conductive gate electrodes of Yu using the two-step silicon deposition process as taught by Balasubramanian to form a low impurity diffusion polysilicon layer within an integrated circuit. (See col.3, lines 6-8).

Regarding the functional limitation: "wherein the two-step silicon deposition process comprises a first step low temperature amorphous silicon deposition process to avoid formation of particles and defects by inhibiting nucleation during the formation of the polysilicon layer, and a second step high temperature polysilicon deposition process", since the two-step deposition of Balasubramanian includes depositing an amorphous silicon (16) on a gate oxide layer (14) at a low temperature, thus, the formation of the amorphous silicon layer (16) of Balasubramanian is inherently result in avoiding the formation of particles and defects by inhibiting nucleation during the formation of the polysilicon layer (18).

With respect to claim 10, the etching process of Yu is a wet etching process.

With respect to claim 11, the wet etching process of Yu utilizes a buffer oxide etchant (BOE).

With respect to claim 12, the cleaning process of Yu is a wet etching process.

With respect to claims 14 and 15,the temperature ranges of the first step low temperature of amorphous silicon (16) deposition process and second step high temperature polysilicon (18) deposition process of Balasubramanian overlaps the claimed range. (See col.6, lines 33-67).

With respect to claim 16, the two-step silicon deposition process of Balasubramanian is performed in single wafer type LPCVD equipment. (See col.11, lines 16-20).

With respect to claim 17, as best understood by the examiner, Yu is shown to teach all the features of the claim with the exception of disclosing the defects includes needle-like defects.

However, in view of Balasubramanian, the two-step deposit of the silicon electrode including deposit amorphous silicon layer (16) on the gate oxide (14) prior to deposit polysilicon layer (18) is inherently result in avoiding formation of particles defects.

Response:

Please refer to the response to the rejection over claims 1, 7 and 8 under 35 U.S.C. 102(b) (item 3), the Applicant believes that claim 9 of the present application is absolutely different from Balasubramanian's disclosure. Reconsideration of the rejection over claim 9 is hereby requested.

As claims 10-12 and 14-17 are dependent upon claim 9, they should be allowed if claim 9 is allowed. Reconsideration of the rejection over claim 9 is therefore requested.

8. Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Balasubramanian '004 and Yu '167 as applied to claims 2 and 9 above, and further in view of Hayakawa (U.S. Patent No. 5,779,520) of record.

Balasubramanian '004 and Yu '167 teach a wet cleaning process utilizing RCA clean. Note that RCA cleaning comprises SC-1 and SC-2.

Thus, Balasubramanian '004 and Yu '167 are shown to teach all the features of the claim with the exception of further utilizing megasonic scrubbing.

However, Hayakawa teaches: cleaning is more effective with physical scrubbing including megasonic scrubbing (See col.2, lines 56-63).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to combine RCA cleaning of Yu with megasonic scrubbing as taught by Hayakawa for utmost effective in removing contaminants.

Response:

As claims 4 and 13 are respectively dependent upon claim 1 and claim 9, they should be allowed if claim 1 and claim 9 are allowed. Reconsideration of the rejection over claims 4 and 13 is therefore requested.

9. Response to Arguments

Applicant's arguments filed July 4, 2003 have been fully considered but they are not persuasive.

With respect to claim 1, contrary to Applicant assertion, the amended claim does not overcome the rejection as indicated.

In response to applicant's argument that "the first step amorphous silicon deposition process **is used to** avoid nucleation of the polysilicon film growth,…so as to inhibit occurrences of needle-like particles and defects on the surface of the polysilicon film", a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235(CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Since the process of Balasubramanian includes depositing the amorphous silicon layer prior to the deposition of the polysilicon layer, the nucleation of the polysilicon film growth is inherently resulted. Further, Applicant clearly indicated that "preventing the occurrence of particles and defects" is achieved by the formation of the α-Si, not the cleaning process.

The process of Balasubramanian anticipates the amended claim.

With respect to claim 9, contrary to Applicant believes, the amended claim is obvious over the teaching of Yu and Balasubramanian.

Response:

Please refer to the response to the rejection over claims

1, 7 and 8 under 35 U.S.C. 102(b) (item 3), the Applicant believes that claim 1 and claim 9 of the present application is absolutely different from Balasubramanian's disclosure. Reconsideration of the rejection over claims 1 and 9 is hereby requested.

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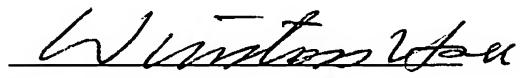

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Winston Hsu, Patent Agent No.41,526
P.O. Box 506
Merrifield, VA 22116
U.S.A.
e-mail:winstonhsu@naipo.com.tw